

What is claimed is:

- 1 1. A system, comprising:
2 a non volatile memory in which is stored an error handling routine, said error
3 handling routine to permit a computer system to continue operating when an error is
4 detected; and
5 a plurality of processors included in the computer system, wherein each
6 processor is capable of accessing the error handling routine on detecting an error
7 and signaling the remaining processors of the plurality of processors to enter a
8 rendezvous state.
- 1 2. The system of claim 1, wherein the error is only correctable by entering the
2 rendezvous state.
- 1 3. The system of claim 1, further comprising a processor abstraction layer
2 located in the non volatile memory, wherein the processor abstraction layer includes
3 the error handling routine.
- 1 4. The system of claim 1, further comprising a system abstraction layer located
2 in the non volatile memory, wherein the system abstraction layer includes the error
3 handling routine.
- 1 5. A system, comprising:
2 a non volatile memory to store an error handling routine and an idle routine,
3 said error handling routine to permit a computer system to continue operating when
4 an error is detected;
5 a plurality of slave processors to execute the idle routine, wherein the
6 plurality of slave processors are included in the computer system; and
7 a monarch processor included in the computer system, the monarch
8 processor being capable of executing the error handling routine to correct the error.

- 1 6. The system of claim 5, wherein the error handling routine is included in a
2 system abstraction layer.
- 1 7. The system of claim 5, wherein the monarch processor is capable of sending
2 a wake up signal to the plurality of slave processors to exit the rendezvous state.
- 1 8. A system, comprising:
2 a plurality of processors including a monarch processor;
3 a processor abstraction layer coupled to the plurality of processors;
4 a system abstraction layer coupled to the processor abstraction layer;
5 an operating system layer coupled to the system abstraction layer; and
6 an interrupt signaling mechanism coupled to the processor abstraction layer,
7 the system abstraction layer, and the operating system layer to initiate a rendezvous
8 state and to end the rendezvous state, said rendezvous state being a state where all of
9 the plurality of processors but the monarch processor are idle.
- 1 9. The system of claim 8, further comprising a system memory and a non
2 volatile memory, wherein the operating system layer is located in the system
3 memory and capable of being executed by the plurality of processors, the processor
4 abstraction layer is located in the non volatile memory and is capable of being
5 executed by the plurality of processors, and the system abstraction layer is located in
6 the non volatile memory and is capable of being executed by the plurality of
7 processors.
- 1 10. The system of claim 8, wherein the monarch processor is capable of
2 executing an error handling routine included in the system abstraction layer upon
3 initiation of the rendezvous state.
- 1 11. The system of claim 8, wherein the processor abstraction layer includes a
2 functional module for error handling.

1 12. A system, comprising:
2 a plurality of processors;
3 a processor abstraction layer located in a non volatile memory coupled to the
4 plurality of processors;
5 a system abstraction layer located in the non volatile memory; and
6 an operating system layer located in a system memory coupled to the
7 plurality of processors to signal all but one of the plurality of processors to end a
8 rendezvous state upon receiving a signal that error handling is completed, said
9 rendezvous state being a state wherein all but the one of said plurality of processors
10 are idle.

1 13. The system of claim 12, wherein the signal from the operating system to end
2 the rendezvous state is an interrupt.

1 14. The system of claim 12, wherein the processor abstraction layer is capable of
2 sending a signal to the system abstraction layer to enter the rendezvous state and
3 performing error handling upon entering the rendezvous state.

1 15. A method, comprising:
2 detecting an error by one processor included in a multiple processor system;
3 entering a rendezvous state in which all processors but the one processor
4 included in the multiple processor system are idle;
5 correcting the error using the one processor; and
6 resuming normal operation.

1 16. The method of claim 15, wherein entering the rendezvous state comprises:
2 requesting a plurality of processors included in the multiple processor
3 system to enter an idle state; and
4 waiting until the plurality of processors have entered the idles state.

1 17. The method of claim 15, further comprising:

2 determining if the error is a severe error; and
3 only upon determining that the error is a severe error, entering the
4 rendezvous state.

1 18. A method, comprising:
2 attempting to correct an error by a detecting processor included in a multiple
3 processor system;
4 on failure, executing firmware code operatively coupled to all the processors
5 included in the multiple processor system to correct the error; and
6 on failure, entering a rendezvous state to correct the error, said rendezvous
7 state being a state where all but one of the processors included in the multiple
8 processor system are idle.

1 19. The method of claim 18, wherein entering a rendezvous state to correct the
2 error comprises:
3 selecting a monarch processor from the processors included in the multiple
4 processor system;
5 signaling slave processors included in the multiple processor system to
6 execute a spin loop; and
7 correcting the error by the monarch processor.

1 20. The method of claim 19, wherein correcting the error by the monarch
2 processor includes executing routines in a processor abstraction layer, a system
3 abstraction layer, and an operating system.

1 21. A method, comprising:
2 attempting to correct an error by a processor included in a plurality of
3 processors;
4 accessing a routine in a first firmware layer to correct the error;
5 selecting a monarch processor included in the plurality of processors;

6 executing a spin loop routine in a second firmware layer by the plurality of
7 processors except the monarch processor;
8 accessing a routine in the second firmware layer to correct the error; and
9 resuming normal operation by the plurality of processors.

1 22. The method of claim 21, wherein selecting a monarch processor comprises
2 determining which processor included in the plurality of processors can best correct
3 the error.

1 23. The method of claim 21, further comprising:
2 determining whether the error is severe.

1 24. An article comprising a machine-accessible medium having associated data,
2 wherein the data, when accessed, results in a machine performing:
3 attempting to correct an error by a detecting processor included in a multiple
4 processor system;
5 on failure, executing firmware code operatively coupled to all the processors
6 included in the multiple processor system to correct the error; and
7 on failure, entering a rendezvous state to correct the error, said rendezvous
8 state being a state where all but one of the processors included in the multiple
9 processor system are idle.

1 25. The article of claim 24, wherein the rendezvous state is a state wherein all
2 but the one of the processors included in the multiple processor system are
3 executing a spin loop.

1 26. The article of claim 24, wherein the data, when accessed, results in the
2 machine performing:
3 informing a processor abstraction layer when all but the one of the
4 processors included in the multiple processor system have entered the idle state.